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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/290,579	04/13/1999	HIDEKI ASADA	OSP-8028	1042

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EXAMINER
ALPHONSE, FRITZ

ART UNIT	PAPER NUMBER
2675	6

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/290,579	ASADA
Examiner	**Art Unit**
Fritz Alphonse	2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 13, 1999*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-89* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☒ Claims *1-89* are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. This application contains claims directed to the following patentably distinct species of the claimed invention:

a) Fig. 1 is directed to species #1 in which the specific element is a MOS type analog amplifier circuit 104, as claimed in claim 1.

b) Fig. 3 is directed to species #2 in which the specific elements are n-type MOS transistor (301) and p-type MOS transistor (302), as claimed in claim 5.

c) Fig. 10 is directed to species # 3 in which the specific elements are a first p-type MOS (1002) and second P-type MOS transistor (1003) with a gate electrode connected to a voltage adjustable power, as claimed in claim 6.

d) Fig. 12 is directed to species # 4 in which the specific element is a second p-type MOS transistor having a gate electrode connected to a voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to a pixel electrode, as claimed in claim 7.

e) Fig. 13 is directed to species # 5 in which the specific element is a second p-type MOS transistor with agate electrode and a source electrode connected to a voltage holding capacitor electrode and a drain electrode connected to a pixel electrode, as claimed in claim 8.

f) Fig. 15 is directed to species # 6 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said n-type MOS transistor and a voltage holding

capacitor electrode; and a resistor connected between said pixel electrode and said voltage holding capacitor electrode, as claimed in claim 15.

g) Fig. 22 is directed to species # 7 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode, and a second n-type MOS transistor having a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to a voltage holding capacitor electrode, and a drain electrode connected to a pixel electrode, as claimed in claim 16.

h) Fig. 24 is directed to species # 8 in which the specific element is a-second n-type MOS transistor having an elelectrode connected to a voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to a pixel electrode, as claimed in claim 17.

I) Fig. 25 is directed to species # 9 in which the specific element is a second n-type MOS transistor with a Gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 18.

j) Fig. 27 is directed to species # 10 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said p-type MOS transistor and a voltage holding capacitor electrode; and a resistor connected between a pixel electrode and a voltage holding capacitor electrode, as claimed in claim 25.

k) Fig. 29 is directed to species # 11 in which the specific elements are a second p-type MOS transistor having a gate electrode connected to a voltage adjustable bias power supply line, a source

electrode connected to a voltage holding capacitor electrode, and a drain electrode connected to a pixel electrode, as claimed in claim 26.

l) Fig. 30 is directed to species # 12 in which the specific elements are voltage holding capacitor electrode; and a second p-type MOS transistor having a gate electrode connected to a voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to a pixel electrode, as claimed in claim 27.

m) Fig. 31 is directed to species #13 in which the specific elements are a second p-type MOS transistor having a gate electrode and a source electrode connected to a voltage holding capacitor, and a drain electrode connected to a pixel electrode, as claimed in claim 28.

n) Fig. 32 is directed to species #14 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said n-type MOS transistor and a voltage holding capacitor electrode, and a resistor connected between said pixel electrode and a voltage holding capacitor electrode, as claimed in claim 35.

o) Fig. 34 is directed to species #15 in which the specific elements are a second n-type MOS transistor having a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to a voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 36.

p) Fig. 35 is directed to species #16 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode; and a second n-type MOS transistor having a gate electrode connected to said

voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode, as claimed in claim 37.

q) Fig. 36 is directed to species #17 in which the specific elements are and a second n-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 38.

r) Fig. 37 is directed to species #18 in which the specific elements are a p-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said n-type MOS-transistor, and one of a source electrode and a drain electrode connected to reset electrode, and another one of the source electrode and the drain electrode connected to a pixel electrode, as claimed in claim 45.

s) Fig. 39 is directed to species #19 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode, and a second p-type MOS transistor with a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 46.

t) Fig. 40 is directed to species #20 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said first p-type MOS transistor and a voltage holding capacitor electrode; and a second p-type MOS transistor with a gate electrode connected to said voltage holding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode, as claimed in claim 67.

u) Fig. 41 is directed to species #21 in which the specific elements are a second p-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 48.

v) Fig. 42 is directed to species #22 in which the specific elements are an n-type MOS transistor having a gate electrode connected to another one of the source electrode and the drain electrode of said p-type MOS transistor, and one of a source electrode and a drain electrode being connected to a reset electrode, and the other of the source electrode and the drain electrode connected to a pixel electrode, as claimed in claim 56.

w) Fig. 44 is directed to species #23 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode; and a second n-type MOS transistor with a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 57.

x) Fig. 45 is directed to species # 24in which the specific elements are a voltage holding capacitor formed between the gate electrode of said first n-type MOS transistor and a voltage holding capacitor electrode; and a second n-type MOS transistor having a gate electrode connected to said voltageholding capacitor electrode, a source electrode connected to a voltage adjustable power supply line, and a drain electrode connected to said pixel electrode, as claimed in claim 58.

y) Fig. 46 is directed to species #25 in which the specific elements are a second n-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to a pixel electrode, as claimed in claim 59.

z) Fig. 47 is directed to species #25 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said second n-type MOS transistor and a voltage holding capacitor electrode; and a resistor connected between said pixel electrode and said voltage holding capacitor electrode, as claimed in claim 67.

A) Fig. 50 is directed to species #26 in which the specific elements are a third n-type MOS transistor with a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 68.

B) Fig. 51 is directed to species #27 in which the specific elements are a third n-type MOS transistor having a gate electrode connected to said voltageholding capacitor electrode, a source electrode connected to a voltage adjustable biaspower supply line, and a drain electrode connected to said pixel electrode, as claimed in claim 69.

C) Fig. 52 is directed to species #28 in which the specific elements are a voltage holding capacitor formed between the gate electrode of said second n-type MOS transistor and a voltage holding capacitor electrode; and a third n-type MOS transistor with a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to said pixel electrode, as claimed in claim 70.

D) Fig. 53 is directed to species # 29in which the specific elements are voltage holding capacitor formed between the gate electrode of said second p-type MOS transistor and a voltage holding capacitor electrode; and a resistor connected between said pixel electrode and said voltage holding capacitor electrode, asclaimed in claim 78.

E) Fig. 56 is directed to species # 31in which the specific elements are a voltage holding capacitor formed between the gate electrode of said second p-type MOS transistor and a voltage holding capacitor electrode; and a third p-type MOS transistor with a gate electrode connected to a voltage adjustable bias power supply line, a source electrode connected to said voltage holding capacity electrode, and a drain electrode connected to a pixel electrode, as claimed in claim 79.

F) Fig. 57 is directed to species #32in which the specific elements are a voltage holding capacitor formed between the gate electrode of said second p-type MOS transistor and a voltage holding capacitor electrode; and a third p-type MOS transistor with a gate electrode connected to said voltage holding capacitor electrode, a source electrode connected to a voltage adjustable bias power supply line, and a drain electrode connected to said pixel electrode, as claimed in claim 80.

G) Fig. 58 is directed to species #33 in which the specific elements are voltage holding capacitor formed between the gate electrode of said second p-type MOS transistor and a voltage holding capacitor electrode; and a third p-type MOS transistor having a gate electrode and a source electrode connected to said voltage holding capacitor electrode, and a drain electrode connected to a pixel electrode, as claimed in claim 81.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, (enter) generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

2. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Conclusion

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703)308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse whose telephone number is (703) 308-8534.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached on (703) 305-9720.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

F. Alphonse

Art Unit: 2675

June 28, 2002

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
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